Proceedings of the 2003 IEEE International Frequency Control Symposium and PDA Exhibition
Jointly with the 17th European Frequency and Time Forum

BROAD TUNING ULTRA LOW NOISE DROs AT 10GHZ UTILISING CERAMIC BASED RESONATORS

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***Abstract* - This paper describes the design of very low noise, tunable, X band Dielectric Resonator Oscillators (DROs) demonstrating phase noise performance of -135dBc/Hz at 10kHz offset.**

A variety of resonator configurations utilising $BaTiO_3$ resonators are presented demonstrating unloaded Qs from 10,000 to 30,000. These resonators are optimally coupled to the amplifiers for minimum phase noise where $Q_L/Q_0 = ½$ and S_{21} = -6dB. SiGe transistors are used for the oscillator sustaining amplifiers which offer reasonable levels of circulating power ~15dBm and gains of 5.4dB per stage as well as low flicker noise corners between 10 and 40kHz. To incorporate tuning, with low additional phase noise, phase shift tuning is incorporated. The theory for the design is included demonstrating close correlation with experimental results.

***Keywords* - Oscillators, phase noise, Dielectric resonator oscillators**

I INTRODUCTION

The best room temperature oscillators currently available typically use sapphire resonators with very sophisticated flicker noise reduction methods [1] (commercially sold by PSI) and more recently using sapphire resonators and SiGe amplifiers [2]. One of the main disadvantages of sapphire at room temperature is the large temperature coefficient (~ -70ppm) thereby requiring sophisticated temperature compensation. This paper presents the design of DROs utilising ceramic based resonators which demonstrate phase noise performance around -135dBc/Hz at 10kHz offset which is close to the predicted minimum. This is typically 25dB better than most commercial designs which use $BaTiO_3$ resonators.

II DESIGN

The design is based on the use of an oscillator arranged in a positive feedback configuration consisting of Silicon Germanium amplifiers, output coupler, varactor diode based phase shifter and high Q $BaTiO_3$ resonator. This is shown in Figure 1.

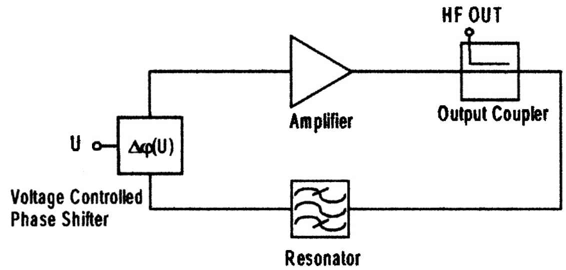

Figure 1 Oscillator configuration

III. PHASE NOISE THEORY

It is important to develop a simple model to calculate and predict the noise performance of an oscillator. A suitable model is shown in figure 1 [3]. This consists of an amplifier with two inputs which are added together. These represent the same input but are separated to enable one to be used for the noise input and the other for feedback. The resonator is represented as an LCR circuit where any impedance transformation is achieved by varying the component values. This circuit operates as a Q multiplication filter but also contains the additional constraint that the AM noise is removed. The model is put in this form to highlight all the effects, which often do not show up in a block diagram model.

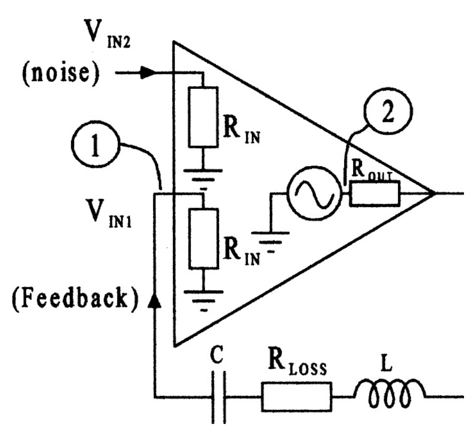

Figure 2 Oscillator model

A general equation for the phase noise can be derived as shown in equation 1 [3] which allows for a number operating conditions including power and the output and input impedances.

Equation 1:

$$L_{FM} = A \cdot \frac{FkT}{8\,(Q_0)^2\,(Q_L/Q_0)^2\,(1-Q_L/Q_0)^N\,P}\left(\frac{f_0}{\Delta f}\right)^2$$

where:

1. N = 1 and A = 1 if P is defined as P_{RF} and R_{OUT} = zero.
2. N = 1 and A = 2 if P is defined as P_{RF} and $R_{OUT} = R_{IN}$.
3. N = 2 and A = 1 if P is defined as P_{AVO} and $R_{OUT} = R_{IN}$.

And P_{RF} is the total power dissipated in the output, input and loss resistances and P_{AVO} is the power available at the output of the amplifier.

If we take expansion 3 and show the full equation [3] we obtain equation 2.

Equation 2:

$$L_{FM} = \frac{FkT}{32 Q_0^{\,2}(Q_L/Q_0)^2(1-Q_L/Q_0)^2 P_{AVO}}\left(\frac{(R_{OUT}+R_{IN})}{R_{OUT}.R_{IN}}\right)\left(\frac{f_0}{\Delta f}\right)^2$$

$$\text{Under optimum conditions} \rightarrow \frac{2FkT}{Q_0^{\,2} P_{AVO}}\left(\frac{f_0}{\Delta f}\right)^2$$

This is minimum when $R_{OUT} = R_{IN}$ and $Q_L/Q_0 = ½$ and hence when the insertion loss of the resonator is –6dB. This minimum occurs because the amplifier gain is set by the insertion loss of the resonator which is $S_{21} = (1-Q_L/Q_0)$. This optimum value for Q_L/Q_0 is also described by Parker in a paper on SAW oscillators [4].

IV AMPLIFIERS

The amplifiers were built with two cascaded SiGe devices. These were resistively biased to arrange for a V_{CE} between 2 to 4 volts and I_C up to 40mA. Circuits were built which both incorporated matching and no matching. For the results shown here no matching was used and gains of 5.4dB per stage were obtained with noise figures around 4dB for two cascaded amplifiers. A typical amplifier circuit is shown in Figure 3 where bias Ts are used to provide bias. Return losses from 15 to 20dB were obtained on the input and output without matching. Additional resistors were added to the bias network to ensure stability – not shown -. To ensure low transposed flicker noise extensive decoupling was incorporated into the supplies. This ties in with work shown in [2]. The frequency response is shown in Figure 4.

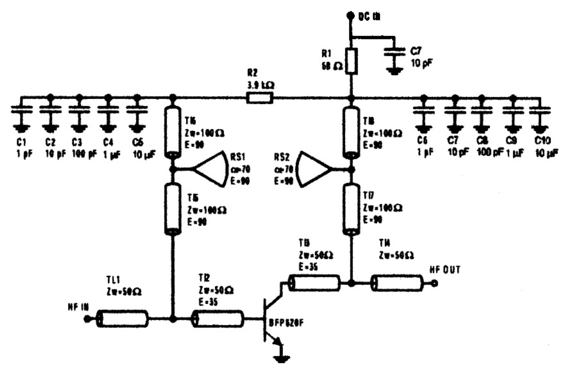

Figure 3 Oscillator sustaining amplifier stages

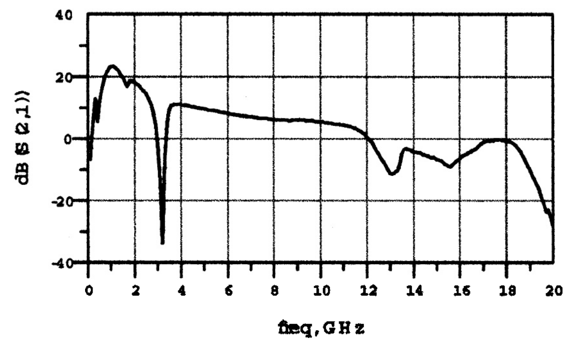

Figure 4 SiGe amplifier frequency response

V RESONATORS

Most DROs are built by mounting the dielectric resonator directly onto microstrip (or with a spacer) and using microstrip coupling lines. The close proximity to the substrate metal and poor symmetry typically limit the loaded Q to a few 100. Further the coupling coefficient is often not optimised for minimum phase noise.

In this paper coaxial coupling, wire coupling and printed loop coupling have been used with the highest Qs being obtained for coaxial coupling. The best dielectric materials have been used with Q factors of 35,000 at 10GHz. The insertion loss set by the coupling loops is set to –6dB for minimum phase noise. The effect of low loss direct mounting to the PCB has also been investigated.

The initial resonator structure is shown in Figure 5 [6] and uses a resonator mounted concentrically in a cylindrical 'cavity'. The resonator is attached to a hollow quartz tube which is sometimes castellated to reduce the contact area. Cyano-acrylate adhesives are used and a jig is used to ensure symmetrical attachment. Unloaded Qs approaching 30,000 have been obtained using this configuration. At this stage it was decided to incorporate printed coupling loops to facilitate ease of design. To obtain the optimum coupling positions and element shape, experiments using a simple wire based coupling element were performed as illustrated in Figure 6. Measurements of Q_L and insertion loss were made for differing wire lengths and angles as illustrated in table 1 and Q_0 was calculated. Once the optimum was found in terms of Q_L and insertion loss, a printed version was then made as illustrated in figure 7 and shown in table 2.

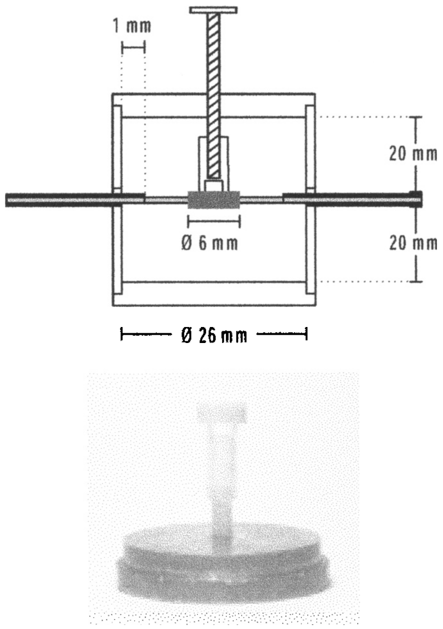

Figure 5 Initial Resonator

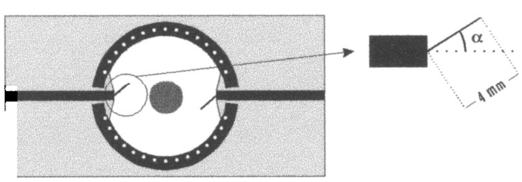

Figure 6 Wire based resonator coupling loops

Table 1 Q_L vs angle

	Measurements	
α	Q_L	S_{21} (db)
0	0	-10.5
22.5	5700	-4.5
45	5500	-3.1
67.5	6500	-4.7
90	10100	-5.6

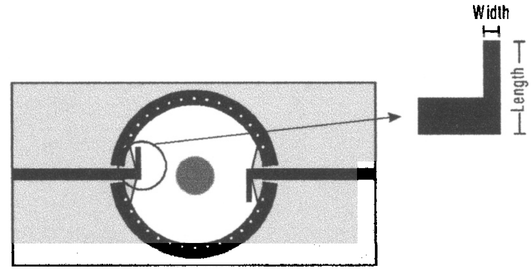

Figure 7 Printed resonator structures

Table 2

Q_L and Q_0 vs element shape

		Length (mm)					
		3		4		5	
		Q_L	S_{21}	Q_L	S_{21}	Q_L	S_{21}
Width (mm)	0.5	0	-30	12,900	-10.1	9,200	-5.2
	0.75	0	-20.7	12,500	-9.6	4,900	-4.5
	1	0	-35.2	11,600	-8.4	6,600	-3.4

One of the problems with the original resonator was that there was an unwanted resonance at 9.21GHz quite close to the wanted resonance. The cavity (metal screen) was therefore made asymmetric vertically which moved the unwanted resonance to 7.68GHz.

As a means to remove the need for a quartz support, experiments were performed to investigate direct mounting of the resonator into the PCB as shown in figure 8. A hole was placed in the centre of the PCB support (no ground plane) and the resonator inserted. The variation of insertion loss Q_L and Q_0 were made vs number of holes. Note that the holes by the loops are not included in the number of holes as these were required for coupling loop adjustment. The results show a reduction in the losses as the number of holes is increased (table 3) due to reduced losses. This is also plotted in figure 9.

Table 3 Q vs number of holes

		Measurement		Calculation
	Holes	S_{21}	Q_L	Q_0
A	0	-6.2dB	3500	6731
B	6	-6.8dB	4766	8665.5
C	16	-6.7dB	5730	10611

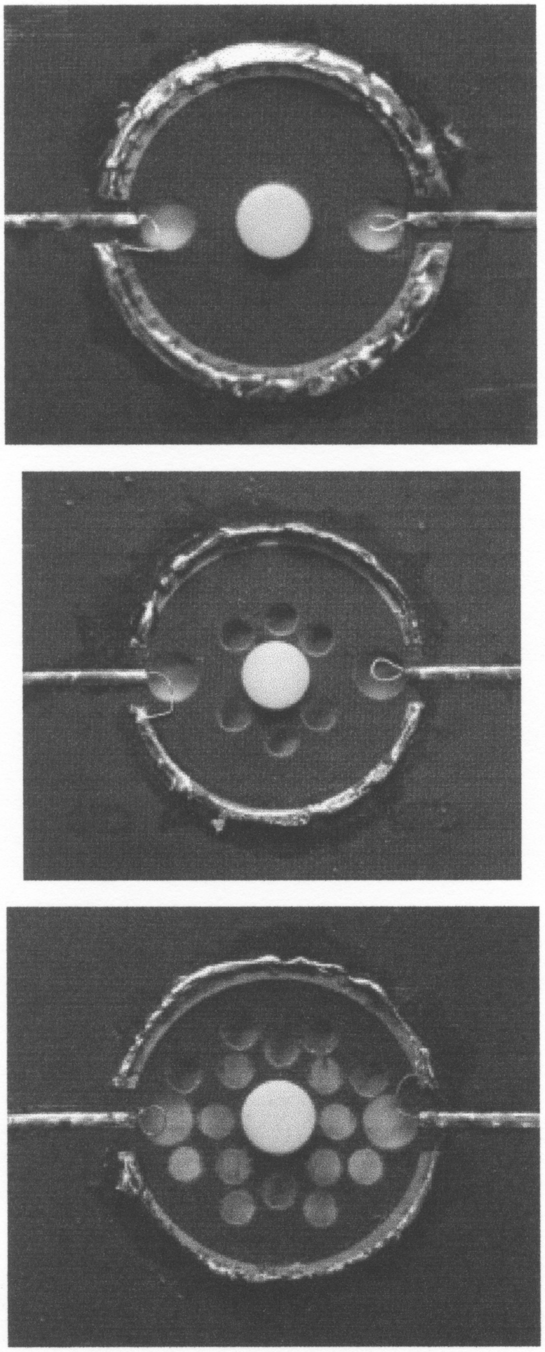

Figure 8 Direct resonator mounting with reduced substrate for increased Q

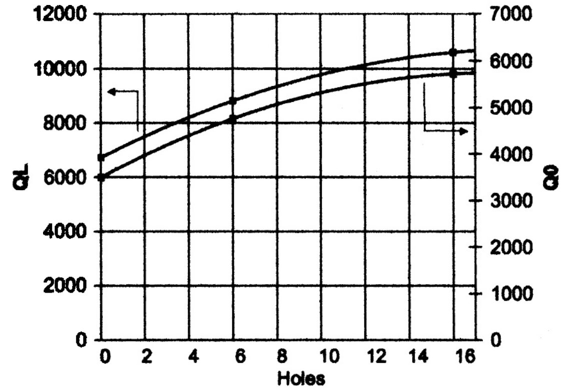

Figure 9 Graph of Q vs number of holes

VI TUNING

To enable narrow band tuning without significant phase noise degradation, an electronic phase shifter network was developed. This enables the resonator and tuning elements to be optimised separately. An oscillator always oscillates at N*360 so adding phase shift moves the oscillation frequency away from the frequency of resonance of the resonator. This changes the loaded Q as the off-resonance Q is proportional to $d\phi/d\omega$. It also changes the resonator insertion loss and hence amplifier gain. The result of this is to produce a $\cos^4\phi$ degradation in phase noise with offset phase. This is illustrated in Figure 6 where measurements were performed on oscillators both in the thermal and flicker noise regime [3] [4].

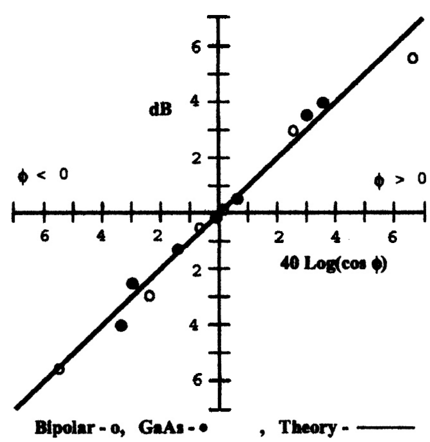

Figure 10. Phase noise degradation with phase noise error

The initial phase shifter consisted of a tunable low pass filter operating well below cut-off as illustrated in Figure 11 where the bias inductors are in fact transmission line bias Ts similar to those used in the amplifiers. However resonances caused by the varactor parasitics (Figure 12) caused very large insertion loss. A high pass configuration was therefore developed as shown in Figure 13. This also has the added advantage of reducing the low frequency closed loop gain in the oscillator. The phase shift variation vs voltage is shown in Figure 14 and the tuning frequency vs voltage is shown in Figure 15.

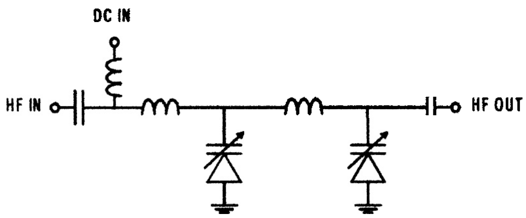

Figure 11 Low pass phase shifter

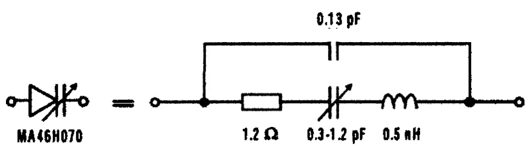

Figure 12 Varactor equivalent circuit

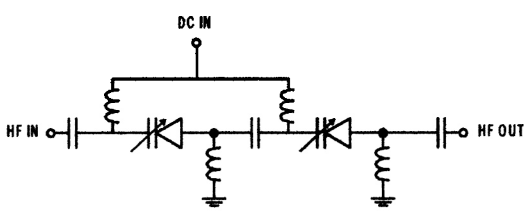

Figure 13 High pass phase shifter

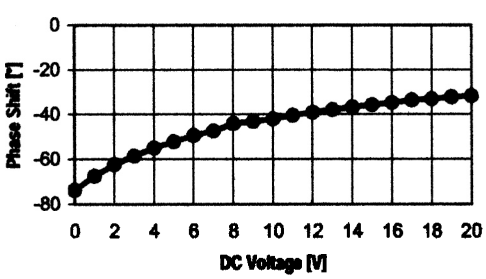

Figure 14 Phase shift vs voltage

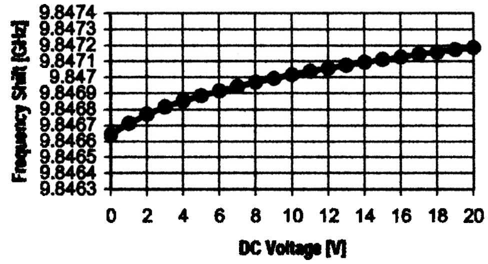

Figure 15 Frequency vs voltage

VII PHASE NOISE MEASUREMENTS

Phase noise measurements were performed using two oscillators and mixing them down to around 22MHz. The phase noise of this beat frequency was then measured using an HP8662 signal generator and HP11729 phase noise measurement system.

A Phase noise plot is shown in Figure 16 with results at 10kHz offset demonstrating a phase noise of −135dBc/Hz. Note the measurement is based on the following parameters.

$$L_{FM\ MEASURED} = \text{Measurement} - \text{BeatNote} - 46dB - 3dB =$$
$$= -92.1dBm/Hz - (-6dBm) - 46dB - 3dB = \underline{-135.1dBc/Hz}$$

A table of the theory for different assumptions for the flicker noise is shown in table 4.

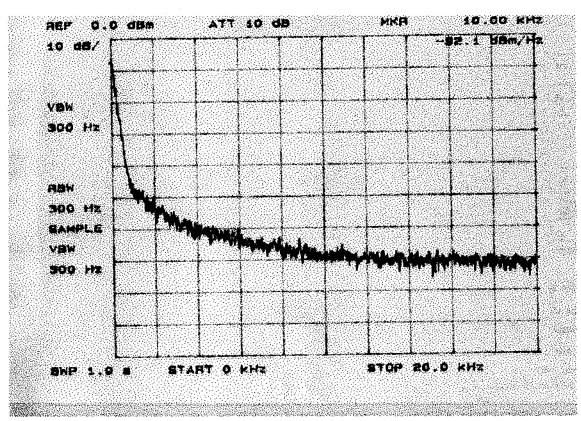

Figure 16 Phase Noise Plot of 10GHz Oscillator

The theoretical sideband phase noise at 10 kHz offset is calculated using the equation shown below assuming:

- A noise Figure F of 5 dB. This is the noise figure of the amplifier, phase shifter and output coupler combined.
- A room temperature T= 290 K

- A resonator with $Q_L = 8200$ with $S_{21} = -5.5$ dB and then $Q_0 = 17400$
- A power available at the output of the amplifier P_{AVO} of 12 dBm

$$L_{FM\ THEORETICAL} = \frac{FkT \cdot \left(1 + \frac{f_C}{\Delta f}\right)}{8 Q_0^2 \left(\frac{Q_L}{Q_0}\right)^2 \left(1 - \frac{Q_L}{Q_0}\right)^2 P_{AVO}} \left(\frac{f_0}{\Delta f}\right)^2$$

The results for different Flicker noise corners are summarised in table 4.

Table 4 Phase noise vs flicker noise corner

f_C [kHz]	$L_{FM\ THEORETICAL}$ [dBc / Hz]
0	-142.6
5	-140.9
10	-139.6
20	-137.9
30	-136.6
40	-135.6

A theoretical phase noise plot vs offset frequency is shown in Figure 17. This includes the flicker noise corner, the far out noise caused by the amplifier and the referred coupler noise.

VIII CONCLUSIONS

High performance low phase noise DROs are demonstrated incorporating a variety of SiGe amplifiers and resonator configurations using BaTiO3 pucks. Very low phase noise is achieved with measured performance of −135dBc/H at 10kHz offset. This is typically 25dB better than most commercial designs. Methods for tuning with low phase noise are described. Accurate prediction and optimisation of phase noise is presented using a 'largely' linear theory is presented.

IX ACKNOWLEDGEMENTS

We wish to thank Infineon for the supply of a large number of Silicon Germanium transistors and MACom for the supply of the varactors diodes.

Phase Noise plots of oscillators in terms of Q0, QL, Power, Noise figure, Carrier frequency, Offset frequency, flicker noise and coupler ratio.

Q0 is the unloaded Q, QL is the loaded Q
F is the noise figure, k is boltzmanns constant, T is the temperature
fo is the carrier frequency, f is the offset frequency, fc is the flicker corner
C0 is is the coupler ratio with respect to the output of the coupler

$Q0 := 17400 \quad QL := 8200 \quad F := 4 \quad T := 293 \quad k := 1.38 \cdot 10^{-23}$

$f0 := 10 \cdot 10^9 \quad fc := 40000 \quad P := .01584 \quad C0 := 10 \quad ORIGIN := 0$

$f := 100, 200 .. 1000000$

$$L(f) := 10 \cdot \log\left[\frac{C0 \cdot F \cdot k \cdot T}{P} + \frac{F \cdot k \cdot T}{2 \cdot P} \cdot \left[\frac{1}{\left(1 - \frac{QL}{Q0}\right)^2}\right] + \frac{F \cdot k \cdot T \cdot \left(1 + \frac{fc}{f}\right)}{8 \cdot (Q0)^2 \cdot \left(\frac{QL}{Q0}\right)^2 \cdot \left(1 - \frac{QL}{Q0}\right)^2 \cdot P} \cdot \left(\frac{f0}{f}\right)^2\right]$$

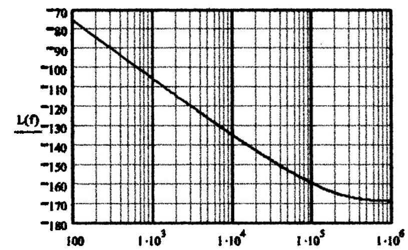

Figure 17. Phase noise plot incorporating flicker noise corner, far out noise and the effect of the coupler

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